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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. WINX-55325
First Inventor or Application Identifier Masaaki Oka
Title PICTURE DRAWING APPARATUS AND PICTURE...
Express Mail Label No. EL691914404US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

- ☒ * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
- ☒ Specification [Total Pages 42]
(preferred arrangement set forth below)
 - Descriptive title of the Invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
- ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 14]
- Oath or Declaration [Total Pages 1]
 - ☐ Newly executed (original or copy)
 - ☒ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
 - ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

- ☐ Microfiche Computer Program (Appendix)
- Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
 - ☐ Computer Readable Copy
 - ☐ Paper Copy (identical to computer copy)
 - ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

- ☐ Assignment Papers (cover sheet & document(s))
- ☐ 37 C.F.R. § 3.73(b) Statement of Power of Attorney (when there is an assignee)
- ☐ English Translation Document (if applicable)
- ☐ Information Disclosure Statement (IDS)/PTO-1449
- ☐ Copies of IDS Citations
- ☒ Preliminary Amendment
- ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
- ☐ * Small Entity Statement(s) filed in prior application, Status still proper and desired (PTO/SB/09-12)
- ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
- ☐ Other:

* NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: 08,930,648
Prior application information: Examiner P. Nguyen Group / Art Unit: 2772

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of)
Masaaki Oka, et al.) Prior Examiner: P. Nguyen
Serial No.) Prior Art Unit: 2772
Filed: Concurrently herewith) Docket No. WINX-55325
For: PICTURE DRAWING) Express Mail No. EL691914404US
APPARATUS AND PICTURE)
DRAWING METHOD)

August 1, 2000
Los Angeles, California 90045

PRELIMINARY AMENDMENT

BOX PATENT APPLICATION
Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This Preliminary Amendment is being filed concurrently with a Rule 53(b)
Continuation application, based upon Serial No. 08/930,648 filed January 20, 1998.

Entry of the following amendments prior to examination of the application is
respectfully requested.

IN THE SPECIFICATION:

IN THE SPECIFICATION:

At page 1, line 1, before the title, please delete "DESCRIPTION".

At page 1, line 2, after the title, please insert:

--Related Applications:

This is a continuation of Serial No. 08/930,648 filed January 20, 1998.--

At page 1, line 3, please change the heading "Technical Field" to --BACKGROUND
OF THE INVENTION--, and between line 3 and 4, please insert the heading:

--Field of the Invention:--.

At page 1, line 11, please change "Background" to --Related--.

At page 4, line 3, please change "Disclosure of the Invention" to --SUMMARY OF
THE INVENTION--.

At page 8, line 14, please change "Best Mode for Carrying Out the Invention" to
--DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS--.

At page 15, line 20, please change "sown" to --shown--.

At page 15, line 21, please change "GLUT" to --GPU--.

At page 16, line 2, please change "GLUT" to --GPU--.

At page 16, line 8, please change "GLUT" to --GPU--.

At page 17, line 10 and 11, please change "33D" to --33F--.

At page 17, line 25, please change "33" to --33F--.

At page 18, line 9, please change "pipeline" to --a pipeline--.

IN THE ABSTRACT:

At page 42, line 1, please change "A picture drawing or method used" to read --The picture drawing method is--.

At page 42, line 2, please delete "For generating".

At page 42, line 3, please change "data required for picture drawing" to read --Data required for picture drawing is generated--.

At page 42, line 5, please delete "generating".

At page 42, line 6, after "pixel data" please insert --is generated--.

At page 42, line 7, please change "frame buffer 18," to --frame buffer 18.--.

At page 42, line 8, please change "the" to --The--.

At page 42, line 12, please delete "the".

At page 42, line 13, please delete "means"; and change "number of times of texture" to read --number of times texture--.

At page 42, line 14, please change "accessing" to --is accessed--.

IN THE CLAIMS:

Please cancel Claims 2-4, without prejudice, and add the following new Claims 5-23:

~~--5.~~ An apparatus comprising:

a processor for generating coordinate data specifying a desired primitive;

a pixel generator for generating pixel data of the desired primitive;

an accessing unit for accessing a memory and storing the pixel data generated by the
5 pixel generator into the memory according to an optimal pixel pattern; and

a control circuit for specifying a shape of the optimal pixel pattern according to the
coordinate data generated by the processor such that the accessing unit stores the pixel data into the
memory with the minimum number of times of accessing the memory.- -

--6. An apparatus according to claim 5, wherein the control circuit specifies the shape
of the optimal pixel pattern by selecting one pixel pattern from a plurality of pixel patterns according
to the coordinate data, the plurality of pixel patterns being different in shape from each other and
each of the plurality of pixel patterns having the same number of pixels.--

--7. An apparatus according to claim 5, wherein the control circuit calculates an
aspect ratio of the desired primitive based on the coordinate data and specifies the shape of the
optimal pixel pattern according to the aspect ratio.--

--8. A video game machine comprising the apparatus according to claim 5.--

~~--9.~~ An apparatus comprising:

a processor for generating coordinate data specifying a desired primitive;

a pixel generator for generating pixel data of the desired primitive;

a control circuit for specifying a shape of a coordinate pattern which has a given size,

5 according to the coordinate data, for dividing a predetermined coordinate area including the

coordinate data in accordance with the coordinate pattern, for detecting at least one coordinate pattern which includes an overlay portion with the desired primitive, and for outputting coordinate pattern information indicating the detected at least one coordinate pattern; and

- an accessing unit for accessing a memory according to the coordinate pattern
- 10 information and for storing the pixel data generated by the pixel generator into the memory in units of pixel data corresponding to the coordinate pattern.--

--10. An apparatus according to claim 9, wherein the control circuit specifies the shape of the coordinate pattern such that the accessing unit stores the pixel data into the memory with the minimum number of times of accessing the memory.- -

--11. An apparatus according to claim 9, wherein the control circuit specifies the shape of the coordinate pattern by selecting one coordinate pattern from a plurality of coordinate patterns according to the coordinate data, the plurality of coordinate patterns being different in shape from each other and each of the plurality of coordinate patterns having the given size.- -

--12. An apparatus according to claim 9, wherein the control circuit calculates an aspect ratio of the desired primitive based on the coordinate data and specifies the shape of the coordinate pattern according to the aspect ratio.- -

--13. An apparatus according to claim 9, wherein the processor determines whether or not the desired primitive is beyond the predetermined coordinate area and, when the desired

primitive is beyond the predetermined coordinate area, the processor divides the desired primitive into a plurality of primitives and executes coordinate transferring of each of the coordinate data
5 corresponding to one of the plurality of primitives such that each of the coordinate data which corresponds to one of the plurality of primitives is included in the predetermined coordinate area, whereby the plurality of primitives are processed successively as the desired primitive.- -

--14. An apparatus according to claim 9, wherein the control circuit outputs the coordinate pattern information which indicates the overlay portion of the detected at least one coordinate pattern.- -

--15. An apparatus according to claim 9, wherein the accessing unit accesses the memory according to the coordinate pattern information and reads the pixel data stored in the memory in units of the pixel data corresponding to the coordinate pattern.- -

--16. A video game machine comprising the apparatus according to claim 9.--

17. A method used in an apparatus which comprises a memory for storing pixel data, the method comprising:

generating coordinate data specifying a desired primitive;

generating pixel data of the desired primitive;

5 specifying a shape of a coordinate pattern which has a given size, according to the coordinate data;

dividing a predetermined coordinate area including the coordinate data in accordance with the coordinate pattern which has a given size;

10 detecting at least one coordinate pattern which includes an overlay portion with the desired primitive;

outputting coordinate pattern information indicating the detected at least one coordinate pattern; and

15 accessing the memory according to the coordinate pattern information and storing the pixel data generated by the pixel generator into the memory in units of pixel data corresponding to the coordinate pattern.--

--18. A method according to claim 17, wherein the step of specifying a shape comprises specifying the shape of the coordinate pattern such that the pixel data is stored into the memory with the minimum number of times of accessing the memory.- -

--19. A method according to claim 17, wherein the step of specifying a shape comprises specifying the shape of the coordinate pattern from a plurality of coordinate patterns according to the coordinate data, the plurality of coordinate patterns being different in shape from each other and each of the plurality of coordinate patterns having the given size.- -

--20. A method according to claim 17, wherein the step of specifying a shape comprises calculating an aspect ratio of the desired primitive based on the coordinate data and specifying the shape of the coordinate pattern according to the aspect ratio.- -

--21. A method according to claim 17, further comprising: determining whether or not the desired primitive is beyond the predetermined coordinate area;

when the desired primitive beyond the predetermined coordinate area, dividing the desired primitive into a plurality of primitives and executing coordinate transferring of each of the coordinate data corresponding to one of the plurality of primitives such that each of the coordinate data which corresponds to one of the plurality of primitives is included in the predetermined coordinate area; and

dealing with the plurality of primitives successively as the desired primitive.- -

--22. A method according to claim 17, wherein the step of outputting coordinate pattern information comprises outputting the coordinate pattern information such that the coordinate pattern information indicates the overlay portion of the detected at least one coordinate pattern.- -

--23. A method according to claim 17, wherein the steps of accessing and storing comprise accessing the memory according to the coordinate pattern information and reading the pixel data stored in the memory in units of the pixel data corresponding to the coordinate pattern.- -

REMARKS

In light of the foregoing amendments, favorable consideration of the application is respectfully requested.

Respectfully submitted,

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Picture Drawing Apparatus and Picture Drawing Method

This invention relates to a picture drawing apparatus and a picture drawing method used in a graphics computer, a special effect device or a video game machine which are a video equipment employing computers.

In a picture generating device in a domestic TV game machine, personal computers or graphics computers, used for generating data of a picture outputted for display to a television receiver, a monitor receiver or a cathode ray tube (CRT) display device, a dedicated drawing device is provided between central processing unit (CPU) and a frame buffer for enabling high-speed processing.

That is, in the above-mentioned picture generating device, the CPU when generating a picture does not directly access the frame buffer, but performs geometry processing, such as coordinate transformation, clipping or light source calculations, defines a three-dimensional model as combination of basic unit figures, such as triangles or quadrangles, in order to formulate a drawing command for drawing a three-dimensional picture, and sends the drawing command thus generated to the drawing device. For generating, for example, a three-dimensional object, the object is resolved into plural polygons and a drawing command for

each polygon is sent from the CPU to the drawing device. The drawing device interprets the drawing command sent from the CPU to execute rendering processing of writing pixel data in the frame buffer, taking into account the Z-values and colors of all pixels making up the polygon, from the Z-values specifying color data and depth of the apex points, for drawing a figure on the frame buffer. The Z-values represent the information specifying the distance from the viewing point along the depth direction.

If, for example, a three-dimensional object is displayed in the above-described picture generating device, the object is resolved into plural polygons, and a drawing command associated with each polygon is transmitted from the CPU to the drawing device. For representing the object more realistically, there are used techniques termed texture mapping or MIP mapping. There are also widely known techniques of converting picture color data via a color lookup table (CLUT) having stored therein color conversion data for changing the display colors.

The texture mapping is a technique of affixing a two-dimensional picture pattern provided separately as a texture source picture to the surface of a polygon constituting the object. The MIP mapping, on the other hand, is among the techniques of texture mapping of interpolating pixel data so that the affixing pattern on the polygon will not be non-spontaneous in case the three-dimensional model is moved towards or away from the viewing point.

Meanwhile, the picture drawing speed depends on the processing speed of texture mapping or MIP mapping for each polygon in a drawing engine. Moreover, the picture drawing speed is influenced by the writing speed from the drawing engine to the frame buffer, such that, if the frame buffer accessing speed is low, the drawing speed is lowered. Therefore, if an expensive high-speed memory is used as a large-capacity frame buffer, for increasing the drawing speed, the system cost is prohibitively increased. However, if an inexpensive dynamic random-access memory (DRAM) is used, the drawing speed of the system is lowered.

In view of the above depicted status of the art, the present invention has for its objects to provide the following.

That is, it is an object of the present invention to provide a picture drawing device and a picture drawing method whereby a high drawing speed may be maintained even with the use of an inexpensive memory, such as DRAM, as a frame buffer.

It is another object of the present invention to provide a picture drawing device and a picture drawing method whereby, in the picture drawing device for executing texture mapping by drawing means, drawing processing can be executed without stopping the drawing means.

It is yet another object of the present invention to provide a picture drawing device and a picture drawing method whereby the number of times of accessing and the accessing time of the

picture memory can be decreased to raise the overall picture drawing speed.

Disclosure of the Invention

A picture drawing apparatus according to the present invention includes pre-processing means for generating data required for drawing processing prior to drawing processing on the unit figure basis in accordance with a drawing command for drawing a picture model defined by the combination of unit figures, picture drawing means for generating pixel data on the unit figure basis by texture mapping processing responsive to the drawing command for drawing a picture on a picture memory, storage means for transient storage of texture data required by the picture drawing means for texture mapping, and supplying means for supplying the texture data required by the picture drawing means for texture mapping to the storage means responsive to data outputted by the pre-processing means.

In the picture drawing device according to the present invention, the picture drawing means has the function of performing MIP mapping, the picture drawing means selecting texture data having the desired resolution responsive to data outputted by the pre-processing means for supplying the selected texture data to the storage means.

A picture drawing method according to the present invention includes the steps of generating data pertinent to picture drawing processing on the unit figure basis in accordance with

a drawing command for drawing a picture model defined by the combination of unit figures, supplying texture data necessary for texture mapping in the picture drawing processing to storage means based on the data, generating pixel data of a unit figure by texture processing for drawing on a picture memory and drawing a picture on a picture memory.

In the picture drawing method according to the present invention, the step of supplying the texture data to the storage means includes a step of supplying texture data of resolution required in MIP mapping in the picture drawing processing responsive to data pertinent to the picture drawing processing.

With the picture drawing device and method according to the present invention, picture drawing means transmit texture data required for texture mapping from a texture memory to a texture cache in a pre-processing stage by the pre-processing means. The pre-processing means and picture drawing means are operated in pipelining for enabling picture drawing without halting the picture drawing means.

With the picture drawing device and method according to the present invention, data of the resolution required for the picture drawing means to perform the MIP mapping is selected from the texture data on the texture memory in the pre-processing stage by the pre-processing means and transmitted to the texture cache for reducing the number of times of accessing and the

accessing time for the texture memory for raising the overall picture drawing speed.

Brief Description of the Drawings

Fig.1 is a block diagram showing the structure of a video game machine embodying the present invention.

Fig.2 is a block diagram showing a detailed structure of a GPU in the video game machine.

Fig.3 is a block diagram showing the basic structure of the GPU.

Fig.4 shows an example of a data structure in a texture cache in the GPU.

Fig.5 is a flowchart showing the processing of resolving a first polygon by a pre-processor in the GPU.

Fig.6 is a block diagram showing the structure of a second bus switcher in the video game machine.

Fig.7 illustrates the structure of a second bus switcher in the video game machine.

Fig.8 illustrates an interleaving pattern to be accessed when having access to the inside of the shape of the first polygon.

Fig.9 illustrates masking in case of for address-based accessing when having access to the inside of the shape of the first polygon.

Fig.10 illustrates the accessing address obtained by the masking.

Fig.12 illustrates an interleaving pattern to be accessed when accessing to the inside of the shape of the second polygon drawn on a memory bank of the frame buffer with a (4×4) interleaving pattern.

Fig.14 illustrates the inside of the second polygon with a (8x2) interleaving pattern.

Fig.15 illustrates an interleaving pattern to be accessed when accessing to the inside of the shape of the second polygon drawn on a memory bank of the frame buffer with a (8×2) interleaving pattern.

Fig.16 illustrates masking in case of address-based accessing to the inside of the shape of the second polygon with a (8x2) interleaving pattern.

Fig.17 illustrates the inside of the second polygon with a (16x1) interleaving pattern.

Fig.18 illustrates an interleaving pattern to be accessed when accessing to the inside of the shape of the second polygon drawn on a memory bank of the frame buffer with a (16×1) interleaving pattern.

Specifically, the present video game device has two sorts of buses, namely a main bus 1 and a sub-bus 2.

To the main bus 1 are connected a central processing unit (CPU) 11, made up of a micro-processor, a main memory 12, made up of a random access memory (RAM), a main dynamic memory access controller or main DMAC 13, a MPEG decoder 14 and a picture processing unit or graphic processing unit (GPU) 15. To the sub-bus 2 are connected a subsidiary central processing unit or sub-CPU 21, made up of a micro-processor, a subsidiary memory, made up of a random access memory (RAM), a subsidiary dynamic memory accessing controller or sub DMAC 23, a read-only memory (ROM) 24, having stored therein a program, such as an operating system, a sound processing unit (SPU) 25, a communication controller or asynchronous transmission mode (ATM) 26, an auxiliary storage device 27, an input device 28 and a CD-ROM driver 30.

The main CPU 11 is a device on the main bus 1 operating by a program on the main memory 12. Since the bus controller 16 is open on start-up, the main CPU 11 reads in a boot program from the ROM 24 on the sub-bus 2 to reproduce the application program and necessary data from the ROM 24 on the sub-bus 1 for loading on the main memory 12 or on devices on the sub-bus 2. On the main CPU 11 is loaded a geometry transfer engine (GTE) 17 for

The main DMAC 13 is a device on the main bus 1 for performing control such as DMA transfer on the devices on the main bus 1. If the bus controller 16 is open, the main DMAC 13 also controls the devices on the sub-bus 2.

The MDEC 14 is an I/O connection device operable in parallel with the main CPU 11 and is a device functioning as a picture

On the sub-bus 2, the sub-CPU 21 is a device on the sub-bus 2 operating in accordance with a program on the sub-memory 22.

The SPU 25 is a device on the sub-bus 2 functioning as a sound processor. This SPU 25 is responsive to a sound command sent as a command packet from the sub-CPU 21 or sub-DMAC 23 as a command packet to read out sound source data from the sound memory 29 to output the read-out data.

The auxiliary storage device 27 is a data input/output device on the sub-bus 2 and is made up of a non-volatile memory, such as a flash memory. This auxiliary storage device 27 temporarily holds on memory data such as game progress or scores.

The input device 28 is an input device from other equipments, such as a control pad on the sub-bus 2, man-machine

receiver or a monitor receiver, not shown.

The packet engine 31 develops the command packet sent from the main CPU 11 or main DMAC 13 shown in Fig.1 over the main bus 1 on a register, not shown.

The pre-processor 32 generates polygon data in accordance with the drawing command sent to the packet engine 31 as command packet and performs pre-set pre-processing, such as polygon division as later explained, on the polygon data, while generating various data such as apex point coordinate information for the respective polygons required by the drawing engine 33, address information such as texture or MIP map texture, or control information, such as pixel interleaving.

The drawing engine 33 includes N polygon engines 33A1, 33A2, ..., 33AN, connected to the pre-processor 32, N texture engines 33B1, 33B2, ..., 33BN, connected to the polygon engines 33A1, 33A2, ..., 33AN, a first bus switcher 33C, connected to the texture engines 33B1, 33B2, ..., 33BN, M pixel engines 33D1, 33D2, ..., 33DM, connected to the first bus switcher 33C, a second bus switcher 33E, connected to the pixel engines 33D1, 33D2, ..., 33DM, a texture cache 33F connected to the second bus switcher 33E, and a CLUT cache 33G connected to the texture cache 33F.

In the drawing engine 33, the N polygon engines 33A1, 33A2, ..., 33AN sequentially generate polygons in accordance with the drawing command on the basis of the polygon data pre-processed

The N texture engines 33B1, 33B2, ..., 33BN perform texture mapping or MIP Mapping in parallel, based on the texture data supplied from the texture cache 33F via color lookup table (CLUT) cache 33G, on each of the polygons generated by the polygon engines 33A1, 33A2, ..., 33AN.

The polygon data, processed with texture mapping or MIP Mapping by the N texture engines 33B1, 33B2, ..., 33BN, are transferred via first bus switcher 33C to M pixel engines 33D1, 33D2, ..., 33DM.

The M pixel engines 33D1, 33D2, ..., 33DM perform various picture processing operations, such as Z-buffer processing or anti-aliasing processing, in parallel, for generating M pixel

In the above-described structure of the GLUT 15, the pre-processor 32 generates the address information for pre-reading the texture affixed to the polygon processed by the N texture engines 33B1, 33B2, ..., 33BN, ..., based on the apex point coordinates [(X0, Y0), (X1, Y1), (X2, Y2)] of the polygons and

the texture coordinates $[(U_0, V_0), (U_1, V_1), (U_2, V_2)]$. In addition, the GLUT 15 reproduces the MIP mapping selection information from the tilt of the sides of the polygons $[(X_1 - X_0)/(Y_1 - Y_0), [(X_2 - X_0)/(Y_2 - Y_0), [(X_1 - X_2)/(Y_1 - Y_2)]$, tilt of the texture addresses $[(U_1 - U_0)/(Y_1 - Y_0), [(U_2 - U_0)/(Y_2 - Y_0), [(U_1 - U_2)/(Y_1 - Y_2), [(V_1 - V_0)/(Y_1 - Y_0), [(V_2 - V_0)/(Y_2 - Y_0), [(V_1 - V_2)/(Y_1 - Y_2), \dots$, or the polygon areas, to furnish the information to the texture cache 33F. The GLUT 15 sorts the polygon apex point coordinates $[(X_0, Y_0), (X_1, Y_1), (X_2, Y_2)]$ in the sequence of the apex points of the left edges $(X_0, Y_0) \rightarrow (X_1, Y_1) \rightarrow (X_2, Y_2)$ or in the sequence of the apex points of the right edges $(X_2, Y_2) \rightarrow (X_1, Y_1) \rightarrow (X_0, Y_0)$ or scans both end points or texture addresses.

The pre-processor 32 stores the information corresponding to the pre-processed polygon data in a work memory, not shown. At a stage in which the drawing engine 33 can process the next polygon, the information capable of processing one polygon is transferred from the work memory to the N polygon engines 33A1, 33A2, ..., 33AN. This causes the drawing engine 33 to start drawing processing for a new polygon.

That is, with the present GPU 15, the pre-processor 32 and the drawing engine 33 executes drawing processing by pipelining processing for drawing a picture defined as the combination of the polygons under a drawing command.

The drawing processing by this pipelining processing is

The pre-processor 32 performs pre-set pre-processing on the polygon data as described above and furnishes various data, such as the apex point coordinate information required by the drawing engine 33, address information for texture or MIP mapping texture or control information, such as pixel interleaving, to the drawing engine 33.

The data structure in the texture cache 33F, shown as an example in Fig.4, is comprised of a tag area TAG made up of texture addresses, a storage area DATA having stored therein the necessary texture data and a flag L specifying that the texture data has not as yet been used. For employing the entry, having the flag L reset, the texture cache 33 reads in the texture data

from the texture area of the frame buffer 18 to set its flag L. The drawing engine 33 reads out the corresponding texture data from the entry, the flag of which has been set, in order to perform drawing processing, and resets the flag 1 of the entry at a stage in which the drawing has come to a close and hence the texture data is no longer required.

In the drawing device, in which the texture mapping processing is carried out as described above, the pre-processor 32 and the drawing engine 33 are constructed as pipeline such that the texture data required by the drawing engine 33 are sent from the texture memory, that is the texture area on the frame buffer 18, to the cache memory 33F at a pre-proceeding stage by the pre-processor 32, so that the drawing processing can be carried out without stopping the drawing engine 33. In addition, by reading only the texture data associated with the resolution required for MIP mapping from the texture area, the number of times of accessing to the texture area can be diminished to raise the drawing speed of the entire device.

The polygon division processing by the pre-processor 32 is carried out in accordance with a flowchart shown in Fig.5.

Specifically, the polygon division processing is started with the polygon count C specifying the number of polygons set to 1.

At a first processing step S1, it is judged whether or not it is necessary to divide a polygon. In the judgment processing

in the processing step S1, it is judged whether or not the polygon now processed is comprised within the range of the texture cache 33F. For this judgment processing, it suffices if calculated values of texture coordinates [(U0, V0), (U1, V1), (U2, V2)] of the apex points of the polygon are within one texture page.

If the result of judgment at the processing step S1 is NO, that is if the polygon needs to be divided, processing transfers to step S2 to perform polygon division by N. Such division by N of the polygon at this processing step S2 is carried out by dividing all sides of the polygon at neutral points, as shown below:

$$X0' = (X0 + X1)/2$$

$$Y0' = (Y0 + Y1)/2$$

$$Z0' = (Z0 + Z1)/2$$

$$X1' = (X1 + X2)/2$$

$$Y1' = (Y1 + Y2)/2$$

$$Z1' = (Z1 + Z2)/2$$

$$X2' = (X2 + X0)/2$$

$$Y2' = (Y2 + Y0)/2$$

$$Z2' = (Z2 + Z0)/2$$

$$U0' = (U0 + U1)/2$$

$$V0' = (V0 + V1)/2$$

$$Z0' = (Z0 + Z1)/2$$

$$U1' = (U1 + U2)/2$$

$$V1' = (V1 + V2)/2$$

$$Z1' = (Z1 + Z2)/2$$

$$U2' = (U2 + U0)/2$$

$$V2' = (V2 + V0)/2$$

$$Z2' = (Z2 + Z0)/2$$

$$R0' = (R0 + R1)/2$$

$$G0' = (G0 + G1)/2$$

$$B0' = (B0 + B1)/2$$

$$R1' = (R1 + R2)/2$$

$$G1' = (G1 + G2)/2$$

$$B1' = (B1 + B2)/2$$

$$R2' = (R2 + R0)/2$$

$$G2' = (G2 + G0)/2$$

$$B2' = (B2 + B0)/2$$

That is, in the division by N of the polygon in the processing step S2, all sides of the polygon are divided at middle points thereof for dividing a triangular polygon, for example, into new polygons with N = 4.

At the next processing step S2, the number of polygons is changed by setting the polygon count C to $C = C+N-1$. Processing then reverts to the first processing step S1 in order to judge whether or not the new as-divided polygons should be sub-divided further. The processing steps S1 to S3 are repeatedly carried out until the new as-divided polygons are comprised within the range of the texture cache.

That is, the pre-processor 32 judges whether or not the polygon now processed in the drawing engine 33 is comprised within the texture cache 33F (judgment condition 1). The pre-processor 32 performs division processing based on the results of judgment for dividing the polygon corresponding to the drawing command so that the new as-divided polygons will be comprised

In this case, it is possible to judge at the first processing step S1 whether or not the MIP map texture referred to by the minimum and maximum values of the Z-values of the apex points of the polygon is traversed (judgment condition 4) and, based on the results of judgement, to divide the polygon corresponding to the drawing command at the processing step S2 into plural polygons in a three-dimensional space for limiting the range of reference of the MIP mapping referred to in a polygon for efficient MIP mapping based on the MIP map texture data read out from the texture cache 33F via the CLUT cache 33G.

It is also possible to judge whether or not the polygon needs to be divided depending on whether or not the number of pixels in a polygon is not more than a pre-set value and to divide the polygon corresponding to the drawing command is not

larger than the prescribed value and to divide the polygon corresponding to the drawing command into plural polygons at the processing step S2 in the three-dimensional space.

It is similarly possible to predict the drawing processing time for the drawing engine 33 based on, for example, the number of pixels in the polygon, judge whether or not the polygon needs to be divided based on whether the pre-processing time by the pre-processor 32 is balanced to the drawing processing time by the drawing engine 33, at the processing step S1 (judgment condition 5) and to divide the polygon corresponding to the drawing command at the processing step S2 based on the result of judgment so that the pre-processing time by the pre-processor 32 is balanced to the drawing processing time by the drawing engine 33. This renders it possible to balance the processing time by the pre-processor 32 and that by the drawing engine 33 relative to each other and to construct the pre-processor 32 and the drawing engine 33 by pipelining to realize high-speed drawing efficiently.

It is also possible to judge at the processing step S1 whether or not the shape of the polygon processed by the processing engine 33 is suited pixel interleaving (judgment condition 6) at the above-mentioned processing step S1 and to divide the polygon corresponding to the drawing command by the processing step S2 into plural new polygons having the shape suitable for the pixel interleaving. This renders it possible to

It is also possible to judge at the processing step S1 whether or not, based on the combination of the judgment conditions 1 and 4, the polygon needs to be divided, and to divide the polygon corresponding to the drawing command by the processing step S2 into plural new polygons so that the new as-divided polygons meet the judgment conditions 1 and 4. This renders it possible to perform MIP mapping processing reliably and efficiently based on texture data read out from the texture cache 33F via CLUT cache 33G. Also, if the judgment conditions 2 and 3 are combined with the above combination, it becomes possible to equate the size of the polygon processed by the drawing engine 33, that is the number of pixels, and to diminish texture distortion.

It is also possible to judge at the processing step S1 whether or not, based on the combination of the judgment conditions 1 and 5, the polygon needs to be divided, and to divide the polygon corresponding to the drawing command by the processing step S2 into plural new polygons so that the new as-divided polygons meet the judgment conditions 1 and 5. This

It is also possible to judge at the processing step S1 whether or not, based on the combination of the judgment conditions 1 and 6, the polygon needs to be divided, and to divide the polygon corresponding to the drawing command by the processing step S2 into plural new polygons so that the new as-divided polygons meet the judgment conditions 1 and 6. This renders it possible to effect texture mapping reliably and efficiently by the drawing engine 33 and to access the frame buffer 18 efficiently to realize high-speed drawing. Also, if the judgment conditions 2 and 3 are combined with the above combination, it becomes possible to equate the size of the polygon processed by the drawing engine 33, that is the number of pixels, and to diminish texture distortion. The judgment condition 4 may also be combined with the above combination to effect MIP mapping or the judgment condition 5 may be combined with the above combination to effect high-speed processing by

pipelining.

The pixel interleaving by the above-mentioned second bus switcher 33E is carried out as described below:

Referring to Fig.6, the second bus switcher 33E includes a control circuit 101 fed with an output of the pre-processor 32 shown in Fig.2, a selector 102 fed with an output of the control circuit 101 and plural multiplexer/demultiplexers (MUX/DMUX) 103a, 103b, 103c, 103d, ... each fed with an output of the selector 102.

The MUX/DMUX 103a, 103b, 103c, 103d, ... are connected to the frame buffer 18 and to the drawing engine 33 shown in Fig.2.

The frame buffer 18 is made up of plural memory banks [1], [2], ..., [X], ..., [L], as shown in Fig.2. Each of the memory banks [1], [2], ..., [X], ..., [L] is made up of a rectangular area represented by 16 addresses (interleaving patterns), so that the 16 addresses can be accessed simultaneously.

Therefore, the memory bank [X], for example, of the frame buffer 18, has 16 input/output ports P_0 to P_{15} for accessing the addresses A_0 to A_{15} . Of the MUX/DMUX 103a, 103b, 103c, 103d, ... , the four MUX/DMUX 103a, 103b, 103c, 103d are each connected to 16 input/output ports P_0 to P_{15} .

Also, the four MUX/DMUX 103a, 103b, 103c, 103d are connected in association with four pixel engines $33D_{x1}$, $33D_{x2}$, $33D_{x3}$ and $33D_{x4}$ of the drawing engine 33.

Since the memory banks other than the memory bank [X] are configured similarly to the above-mentioned memory bank [X], the detailed description therefor is not made for simplicity. The accessing operation performed by the second bus switcher 33E on the other memory banks is similar to that performed by the second bus switcher 33E on the memory bank [X] as later explained. Therefore, in the following description, only the accessing operation performed by the second bus switcher 33E on the memory bank [X] is explained.

First, a series of operations by the second bus switcher 33E is explained.

If, for example, the shape of a polygon drawn on the memory bank [X] is a triangle T_{ABC} (the shape of the first polygon) as shown in Fig.7, the control circuit 101 is first fed from the pre-processor 32 with the pixel interleaving control information. Based on the pixel interleaving control information from the pre-processor 32, the control circuit 101 changes over an interleaving pattern, used for accessing the inside of the triangle T_{ABC} , to, for example, a (4×4) interleaving pattern.

The method for changing over the interleaving pattern in the control circuit 101 will be later explained in detail.

Of plural interleaving patterns formed on the memory bank [X], such interleaving pattern to be accessed, that is, such interleaving pattern as permits the inside of the triangle T_{ABC} to be accessed in its entirety, is detected by the control

circuit 101, with the aid of the (4×4) interleaving pattern.

Thus, in the triangle T_{ABC} , if each interleaving pattern on the memory bank [X] is indicated by P (pattern index in the x-direction and pattern index in the y-direction), a sum total of 20 interleaving patterns specified by

$$\begin{aligned}
 P(x,y) = & P(3,1), P(4,1), P(1,2), \\
 & P(2,2), P(3,2), P(4,2), \\
 & P(1,3), P(2,3), P(3,3), \\
 & P(4,3), P(5,3), P(2,4), \\
 & P(3,4), P(4,4), P(5,4), \\
 & P(3,5), P(4,5), P(5,5), \\
 & P(4,6), P(5,6)
 \end{aligned}$$

are detected, as shown in Fig.8.

The control circuit 101 routes the pattern information specifying the 20 interleaving patterns, detected as described above, to the selector 102 on the interleaving pattern basis. When performing memory accessing on the address basis, the control circuit 101 routes the mask information corresponding to the shape of the triangle T_{ABC} to the selector 102.

Based on the pattern information, supplied from the control circuit 101 on the interleaving pattern basis, the selector 102 designates the address corresponding to the (4×4) interleaving pattern P to be accessed for the MUX/DMUX 103a, 103b, 103c and 103d.

If fed with the mask information from the control circuit

15 101, the selector 102 designates for MUX/DMUX 103a to 103d the accessing addresses obtained as a result of masking performed in the (4×4) interleaving patterns P, on the basis of the masking information, as shown in Fig.9. Thus, of the addresses A_0 to A_{15} in the interleaving pattern specified by P(4,1) shown in Fig.9, the addresses to be accessed, obtained as the result of masking, are A_4 , A_5 , A_6 , A_8 , A_9 , A_{10} , A_{13} , A_{14} and A_{15} , shown shaded in Fig.10.

The MUX/DMUX 103a, 103b, 103c and 103d access the addressees A_0 to A_{15} on the memory bank [X] designated by the selector 102.

The pixel engines $33D_{x1}$, $33D_{x2}$, $33D_{x3}$ and $33D_{x4}$ output pixel data to the MUX/DMUX 103a, 103b, 103c and 103d, respectively, as explained previously.

Thus the MUX/DMUX 103a accesses the address designated by the selector 102 to write pixel data from the pixel engine X_a , via one of the input/output ports P_0 to P_{15} corresponding to the address designated by the selector 102, in an area on the memory bank [X] designated by the above address.

The MUX/DMUX 103a accesses the address designated by the selector 102 to read out data written in an area designated by the address on the memory bank [X] via one of the input/output ports P_0 to P_{15} corresponding to the above address. The MUX/DMUX 103a performs pre-set processing on the data read out from the memory bank [X].

The method for changing over the interleaving patterns in the above-described control circuit 101 is now specifically explained.

In this case, the interleaving patterns to be accessed are:

totaling at 17, as shown in Fig.12

In case of accessing on the address basis, only the required memory addresses can be accessed by carrying out the masking in

the (4×4) interleaving pattern P , as in case of accessing the above-mentioned triangle T_{ABC} , as shown in Fig.13

Then, if the inside of the triangle T_{DEF} is accessed with a (8×2) interleaving pattern P_1 as shown in Fig.14, the interleaving patterns to be accessed are

$$\begin{aligned}
 P_1(x,y) = & P_1(1,2), P_1(2,2), \\
 & P_1(0,3), P_1(1,3), \\
 & P_1(2,3), P_1(0,4), \\
 & P_1(1,4), P_1(2,4), \\
 & P_1(3,4), P_1(1,5), \\
 & P_1(2,5), P_1(3,5), \\
 & P_1(4,5), P_1(3,6), \\
 & P_1(4,6)
 \end{aligned}$$

totaling at 15, as shown in Fig.15.

That is, if the inside of the triangle T_{DEF} is accessed with the (8×2) interleaving pattern, the number of times of accessing required for accessing the entire inside of the triangle T_{DEF} is 15.

In case of accessing on the address basis, masking is performed within the (8×2) interleaving pattern P_1 as in case of accessing the triangle T_{ABC} as described above, as shown in Fig.16, for accessing only the needed memory address.

Then, if the inside of the triangle T_{DEF} is accessed with a (16×1) interleaving pattern P_2 , as shown in Fig.17, the interleaving patterns to be accessed are

$$\begin{aligned}
P_2(x,y) = & P_2(0,5), P_2(1,5), \\
& P_2(0,6), P_2(1,6), \\
& P_2(0,7), P_2(1,7), \\
& P_2(0,8), P_2(1,8), \\
& P_2(0,9), P_2(1,9), \\
& P_2(0,10), P_2(1,10), \\
& P_2(2,10), P_2(1,11), \\
& P_2(2,11), P_2(1,12), \\
& P_2(2,12), P_2(2,13)
\end{aligned}$$

totaling at 18, as shown in Fig.18.

That is, if the inside of the triangle T_{DEF} is accessed with the (16×1) interleaving pattern, the number of times of accessing required for accessing the entire inside of the triangle T_{DEF} is 18.

In case of accessing on the address basis, masking is performed within the (8×2) interleaving pattern P_2 as in case of accessing the triangle T_{ABC} as described above, as shown in Fig.19, for accessing only the needed memory address.

As described above, the number of times of accessing the inside of the triangle T_{DEF} with the (4×4) interleaving pattern P is 17, while that of accessing the inside of the triangle T_{DEF} with the (8×2) interleaving pattern P_1 is 15 and that of accessing the inside of the triangle T_{DEF} with the (16×1) interleaving pattern P_2 is 18. Thus, the number of times of accessing the inside of the triangle T_{DEF} with the (8×2)

interleaving pattern P_1 represents the minimum number of times of accessing. Thus it is seen that a proper interleaving pattern for the triangle T_{DEF} is the (8×2) interleaving pattern P_1 .

Thus, for switching the interleaving pattern used for accessing the memory bank [X] to a proper interleaving pattern in meeting with the shape of the polygon to be accessed, the control circuit 101 executes the following processing operations.

If, for example, the shape of a polygon drawn on the memory bank [X] is a triangle T_{HIJ} , as shown in Fig.20, the control information for pixel interleaving is supplied from the pre-processor 32 to the control circuit 101, as described above. For example, the control information for pixel interleaving is such information as xy coordinates H (X_h, Y_h), I (X_i, Y_i) or J (X_j, Y_j) of three apex points of the triangle T_{HIJ} .

The control circuit 101 then finds, using the control information for pixel interleaving from the pre-processor 32, the aspect ratio R of the triangle T_{HIJ} , by calculations:

$$\begin{aligned} R &= dy/dx \\ &= (MAXy - MINy)/(MAXx - MINx) \end{aligned}$$

where MAXx and MINx are maximum and minimum values in the X-direction, respectively, and MAXy and MINy are maximum and minimum values in the Y-direction, respectively, as shown in Fig.20.

In the triangle T_{HIJ} ,

$$\text{MAXx} = \text{Xj}$$

$$\text{MINx} = \text{Xi}$$

$$\text{MAXy} = \text{Yh}$$

$$\text{MINy} = \text{Yi}$$

Depending on the aspect ratio R , thus found, the control circuit 101 selects one of five interleaving patterns Pa to Pe of (1×16) , (2×8) , (4×4) , (8×2) and (16×1) , as shown in Fig.21, and switches the interleaving pattern used in accessing the inside of the triangle T_{HIJ} to the selected interleaving pattern.

The control circuit 101 has a table for the aspect ratio R and interleaving patterns (Table 1). In this table are pre-set proper interleaving patterns associated with various values of the aspect ratio R , that is such an interleaving pattern as minimizes the number of times of accessing. Thus the control circuit 101 selects, using the above table, a proper interleaving pattern associated with the aspect ratio R found as described above.

TABLE 1

aspect ratio R	interleaving pattern
~ 0.1	$\text{Pa } (16 \times 1)$
$0.1 \sim 0.5$	$\text{Pb } (8 \times 2)$
$0.5 \sim 2.0$	$\text{Pc } (4 \times 4)$
$2.0 \sim 8.0$	$\text{Pd } (2 \times 8)$
$8.0 \sim$	$\text{Pe } (1 \times 16)$

That is, the present video game machine 201 is basically made up of a main body member 202 and an operating device 217 connected to the main body member 202 via a cable 227, as shown in Fig.22. At a mid portion on the upper surface of the main body member 202 is mounted a disc loading unit 203 within which is loaded a CD-ROM 251 shown in Fig.25. On the left side of the disc loading unit 203 are mounted a power source switch 205 operated for turning on or off the device and a reset switch 204 operated for transiently resetting the game. On the right side of the disc loading unit 203 is mounted a disc actuating switch 206 operated

for mounting or dismounting the CD-ROM 251 with respect to the disc loading unit 203.

On the front side of the main body member 202 are mounted connecting portions 207A, 207B, as shown in Fig.23. These connecting portions 207A, 207B are provided with a connection terminal 226 provided on the foremost part of the cable 227 derived from the operating device 217 and a connection terminal inserting portion 212 for connecting a recording device 228, such as a memory card, and a recording/inserting portion 208. That is, two each of the operating devices 217 and recording devices 228 can be connected to the main body member 202.

The front view of Fig.23 shows the state in which the connection terminal portion 226 and the recording device 228 are loaded on the right side connecting portion 207B with none of the connecting terminal portion 226 nor the recording device 228 being loaded on the left side connecting portion 207A. The recording inserting portion 208 for loading the recording device 228 thereon is provided with the shutter 209, as shown in Fig.23. When loading the recording device 228 on the main body member 202, the shutter 209 is thrust by the foremost part of the recording device 228 to effect loading.

The connecting terminal portion 226 has a knurled gripping part 231A for anti-slip effect. Similarly, the recording device 228 has a knurled gripping part 242A for anti-slip effect. Referring to a side view of Fig.24, the connecting terminal

The operating device 27 has supports 220, 221 that can be gripped with left and right hands. The foremost parts of the supports 220, 221 are provided with operating parts 218, 219, respectively. The operating parts 224, 225 are operated with index fingers of both hands, while the operating parts 218, 219 are operated with thumbs of both hands.

With the present video game machine 201, the CD-ROM 251 loaded on the disc loading unit 203 is reproduced by the CD-ROM driver 30. The operating device 217 is equivalent to the above-mentioned input device 28, while the recording device 228 is equivalent to the auxiliary storage device 27.

CLAIMS

1. A picture drawing apparatus comprising:
- pre-processing means for generating data required for drawing processing prior to drawing processing on the unit figure basis in accordance with a drawing command for drawing a picture model defined by the combination of unit figures;
- picture drawing means for generating pixel data on the unit figure basis by texture mapping processing responsive to said drawing command for drawing a picture on a picture memory;
- storage means for transient storage of texture data required by the picture drawing means for texture mapping; and
- supplying means for supplying the texture data required by said picture drawing means for texture mapping to said storage means responsive to data outputted by said pre-processing means.
2. The picture drawing device as claimed in claim 1 wherein said picture drawing means has the function of performing MIP mapping, said picture drawing means selecting texture data having the desired resolution responsive to data outputted by said pre-processing means for supplying the selected texture data to said storage means.
3. A picture drawing method comprising the steps of:
- generating data pertinent to picture drawing processing on the unit figure basis in accordance with a drawing command for drawing a picture model defined by the combination of unit

supplying texture data necessary for texture mapping in said picture drawing processing to storage means based on said data;

4. The picture drawing method as claimed in claim 3 wherein said step of supplying said texture data to said storage means includes a step of supplying texture data of resolution required in MIP mapping in said picture drawing processing responsive to data pertinent to said picture drawing processing.

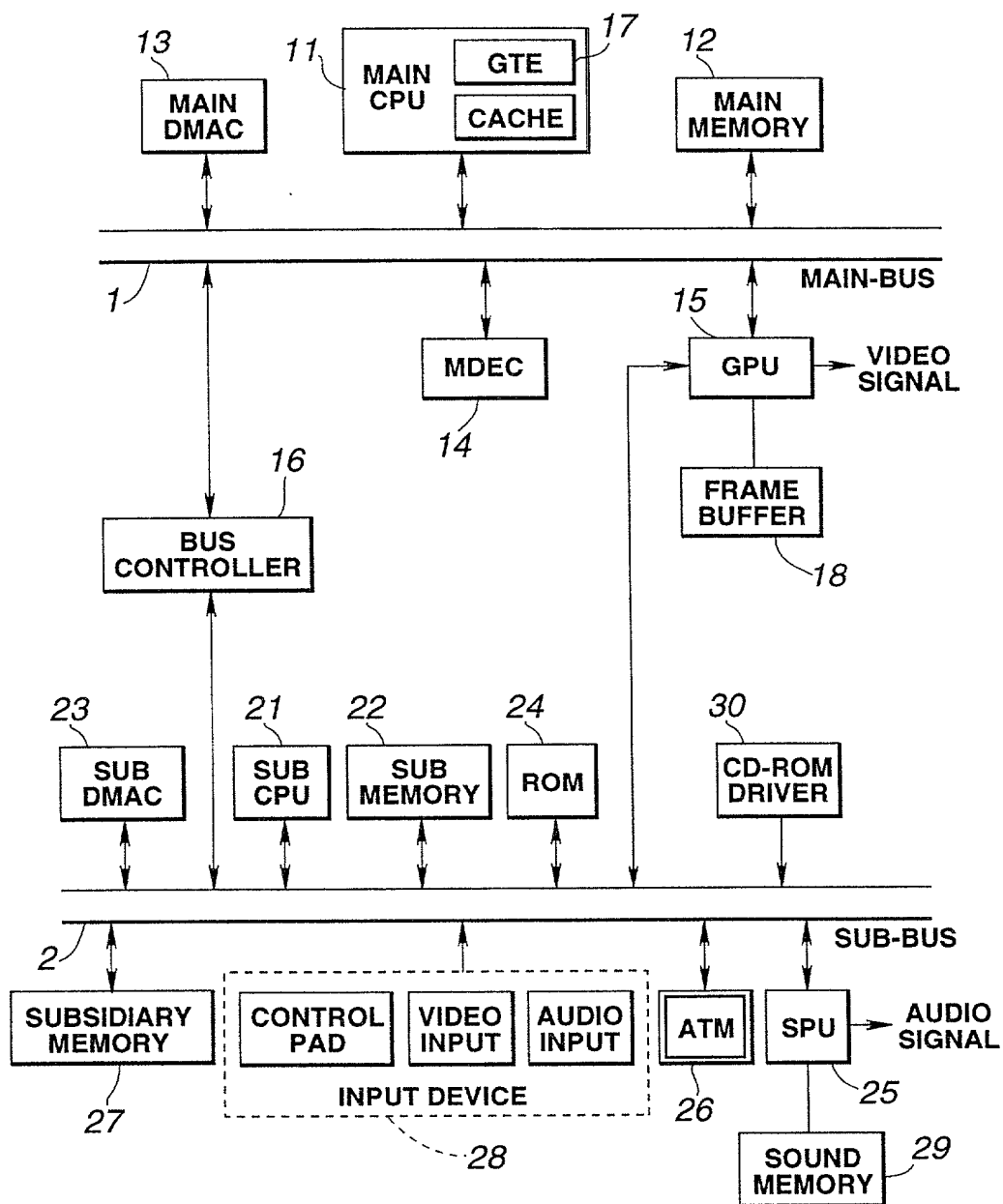


FIG.1

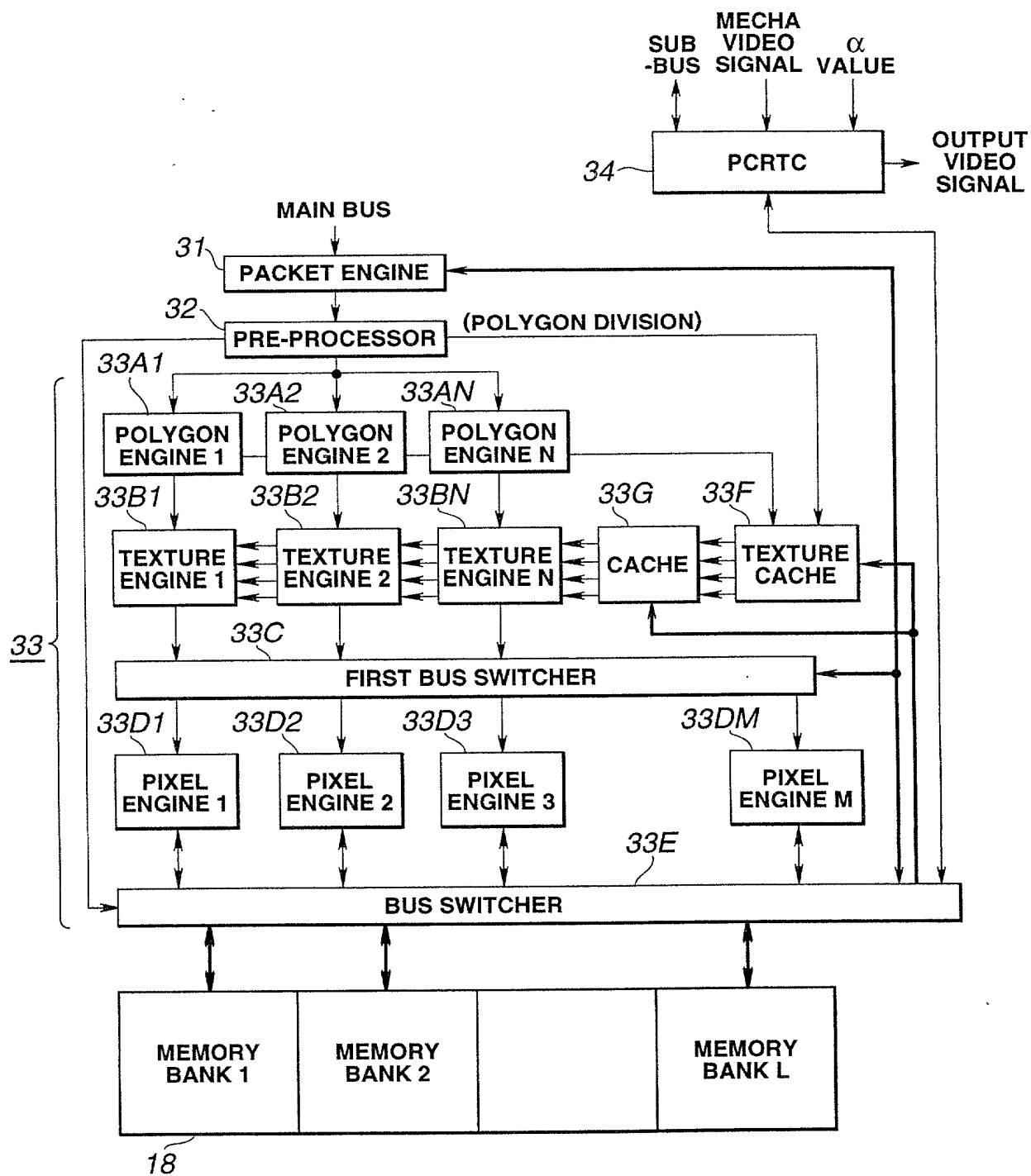


FIG.2

FIG.3



FIG.4

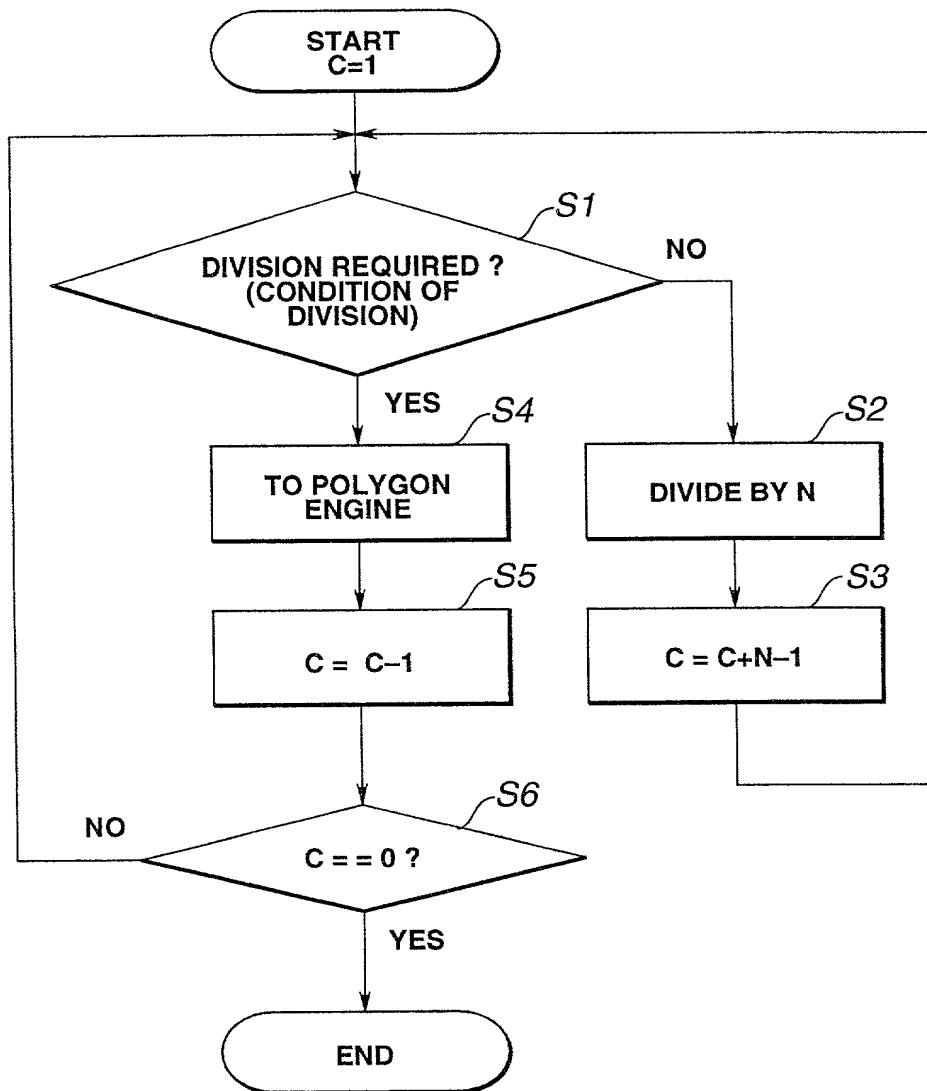


FIG.5

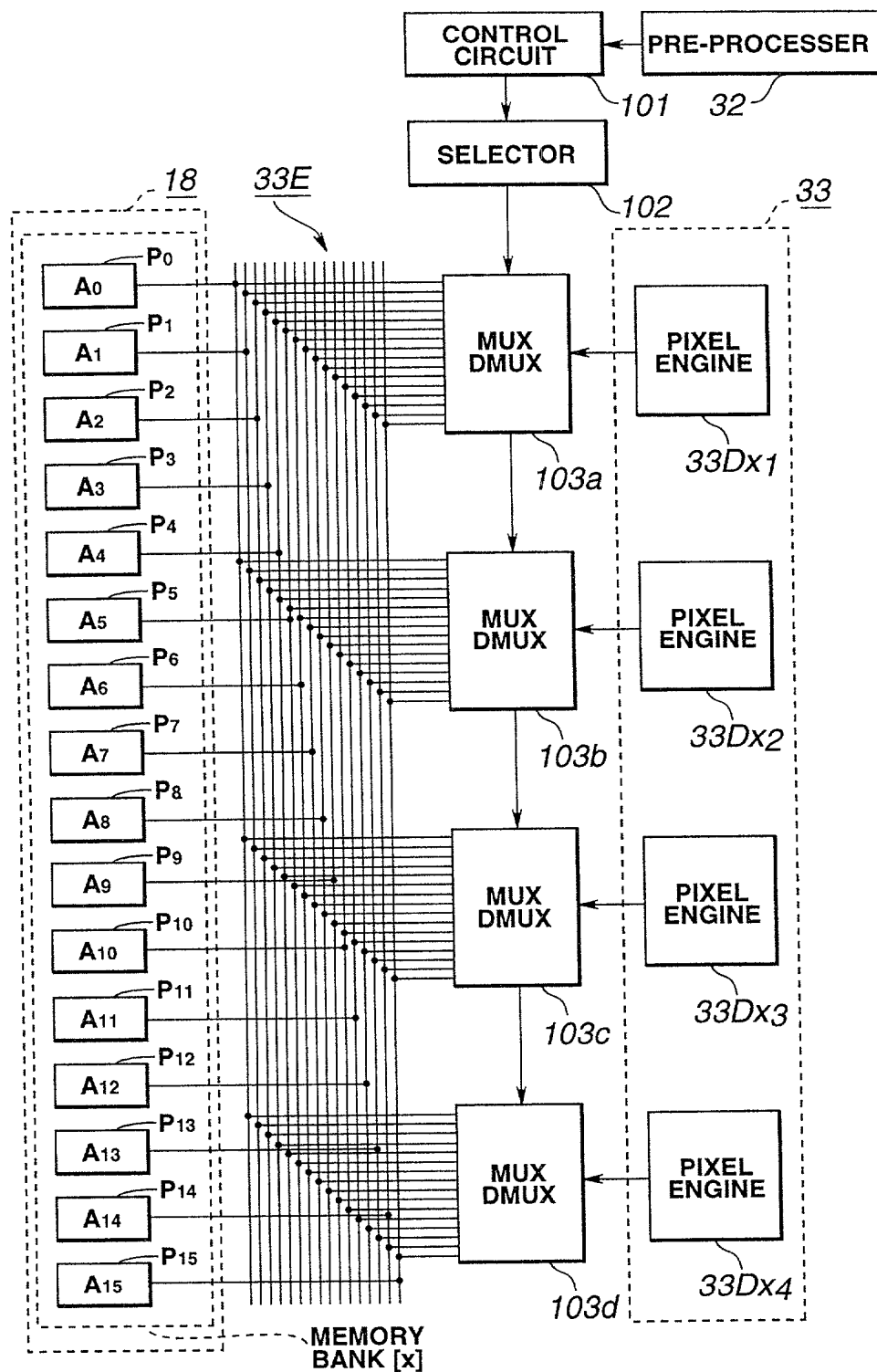


FIG.6

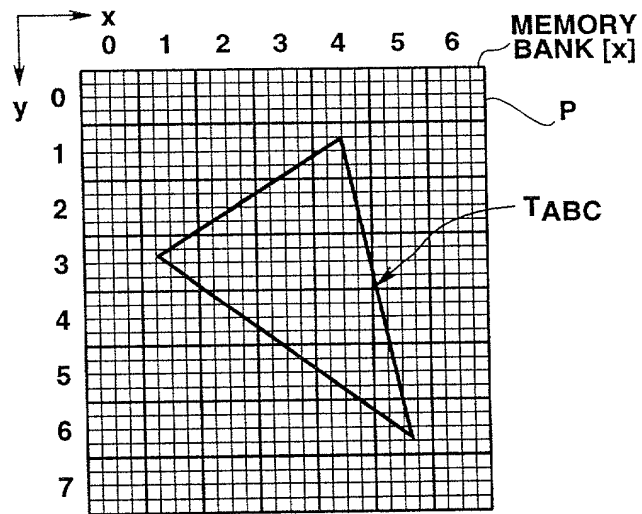


FIG. 7

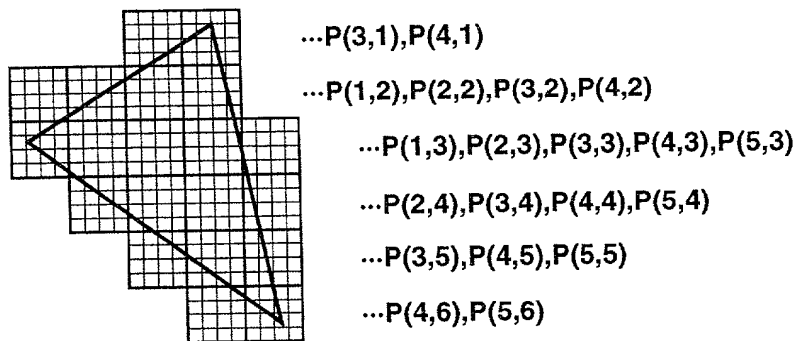


FIG. 8

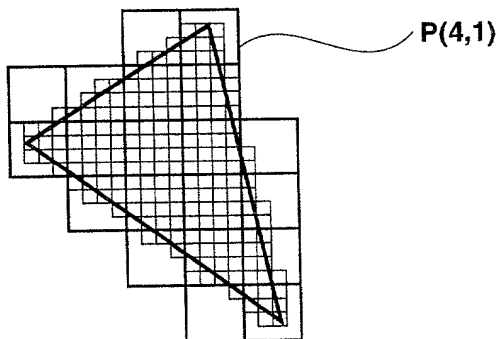


FIG. 9

$P(4,1)$

	A0	A1	A2	A3	A0	. . .
	A4	A5	A6	A7	A4	. . .
	A8	A9	A10	A11	A8	. . .
	A12	A13	A14	A15	A12	. . .
	A0	A1	A2	A3	A0	. . .
	
	

FIG.10

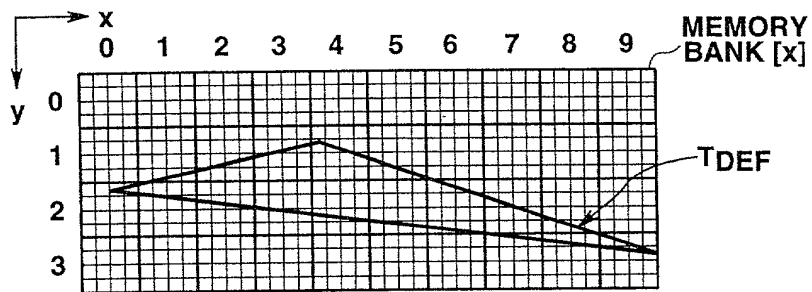


FIG.11

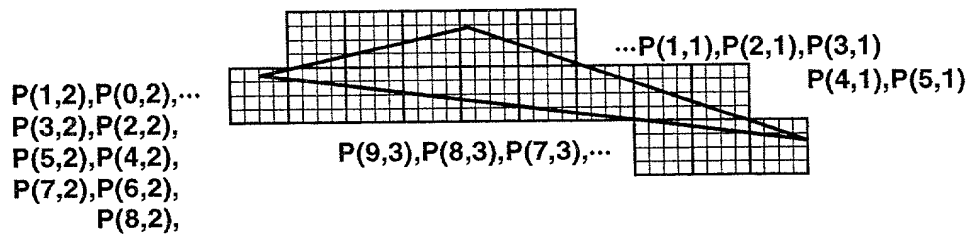


FIG.12

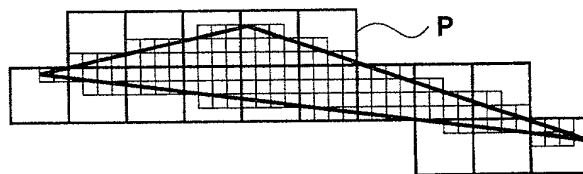


FIG.13

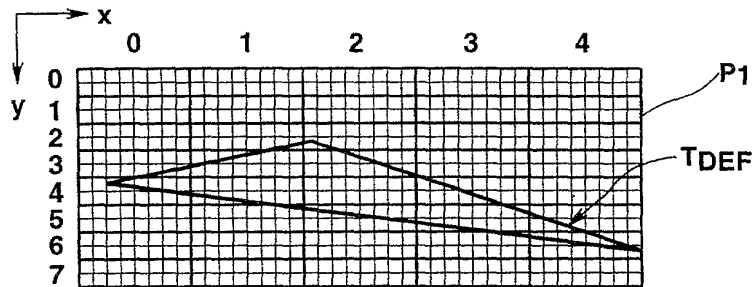


FIG. 14

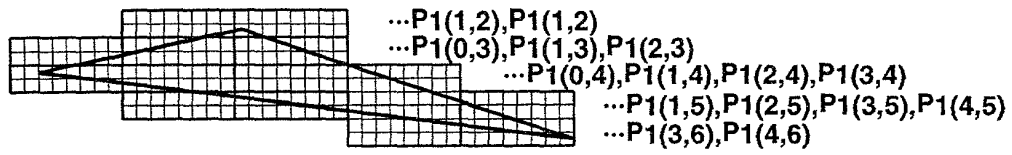


FIG. 15

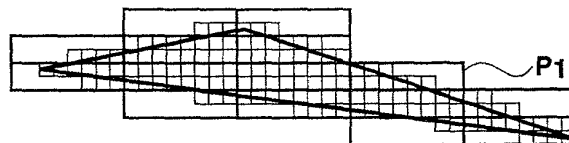


FIG. 16

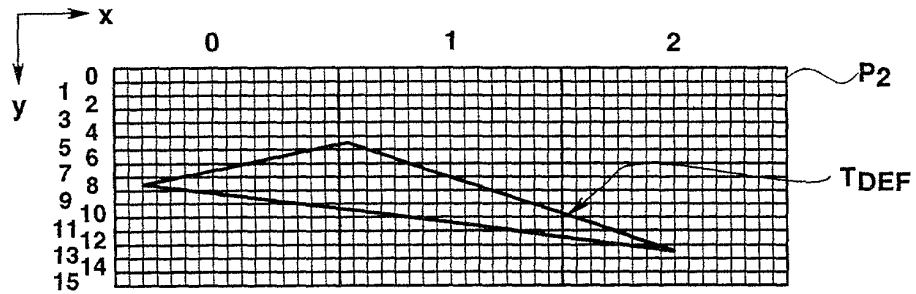


FIG.17

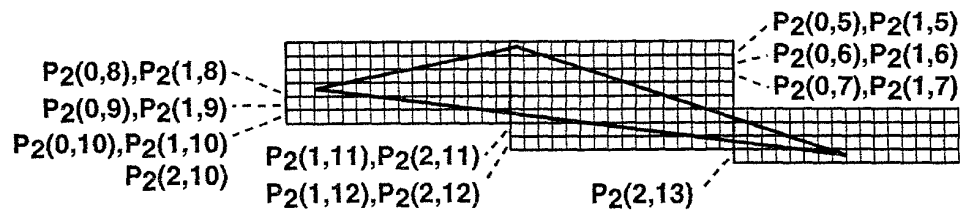


FIG.18

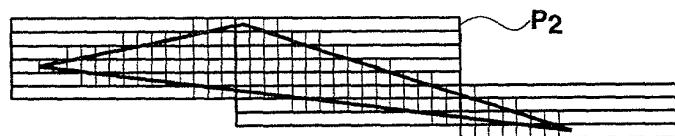


FIG.19

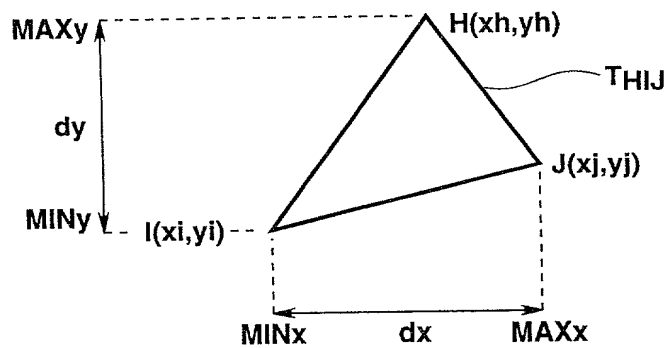


FIG.20

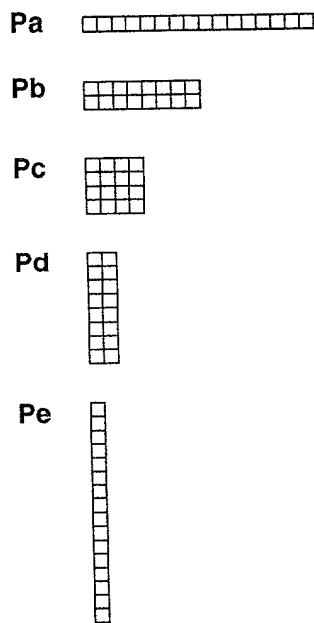


FIG.21

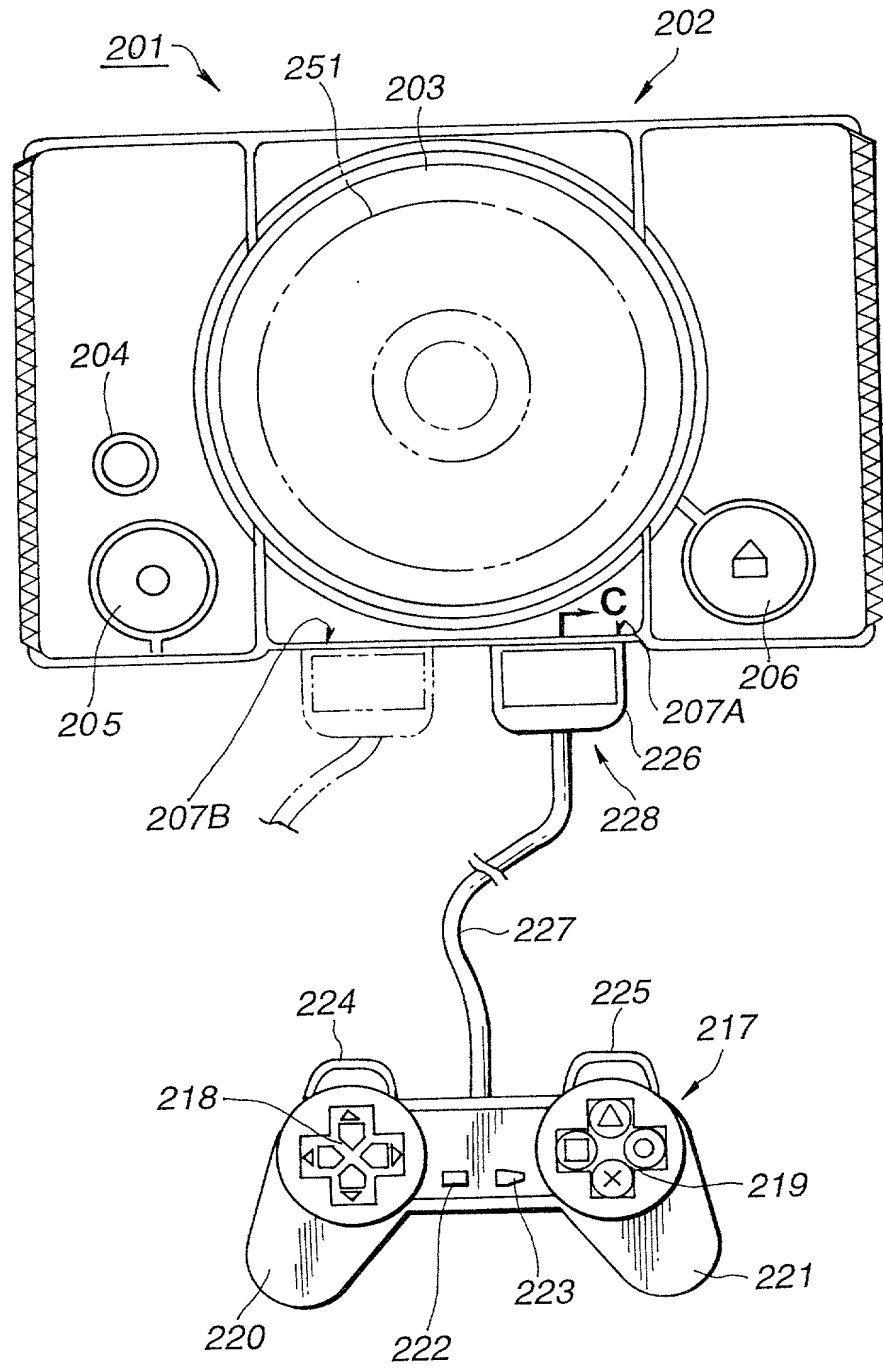


FIG.22

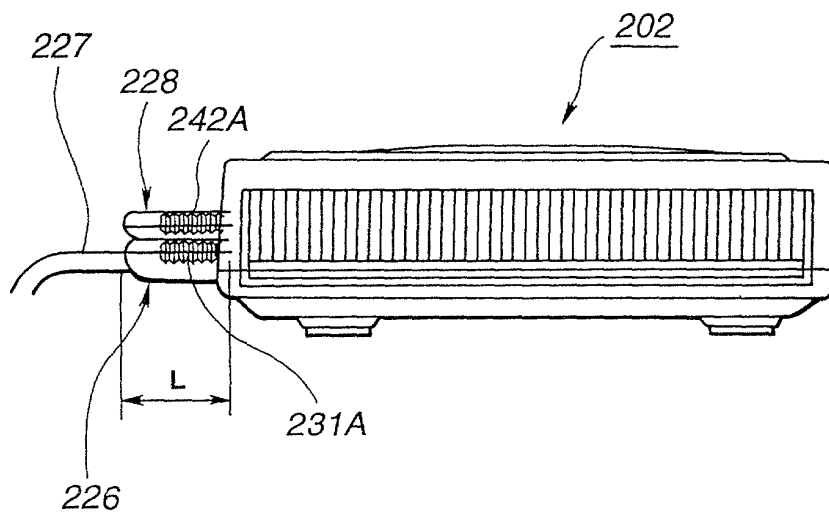


FIG.24

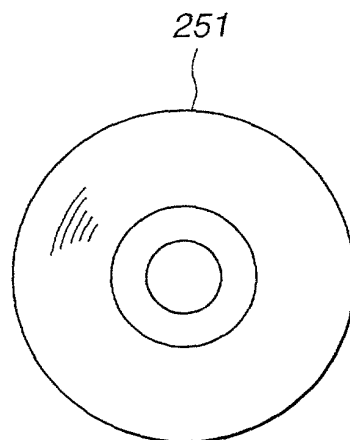


FIG.25

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name:

I verily believe I am the original, first and sole inventor (if only one name is listed below at 201) or a joint inventor (if plural inventors are named below at 201-203) of the invention

entitled Picture Drawing Apparatus and Picture Drawing Method

which is described and claimed in

International application No. PCT/JP97/00297 filed February 06, 1997 and as amended

on _____ (if any), which I have reviewed and for which I solicit a patent;

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to my international application.

I do not know and do not believe that the invention was in public use or on sale in the United States of America more than one year prior to said earlier application.

I hereby state that the invention has not been patented or made the subject of an inventor's certificate issued before the date of my international application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to my international application.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority Claimed

(Number)	(Country)	(Day)	(Month)	(Year Filed)	Yes	No
JP8-020332	Japan	06	02	96	X	
(Number)	(Country)	(Day)	(Month)	(Year Filed)	Yes	No
(Number)	(Country)	(Day)	(Month)	(Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status)	(patented, pending, abandoned)
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(Application Serial No.)	(Filing Date)	(Status)	(patented, pending, abandoned)
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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Messrs.

**See Below

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 201	Signature of Inventor 202	Signature of Inventor 203
Date	Date	Date

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